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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/556,398	11/10/2005	Francois Droz	90500-000067/US	6278

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EXAMINER	
MAI, THIEN T	

ART UNIT	PAPER NUMBER
2887	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/556,398	DROZ, FRANCOIS	
	Examiner	Art Unit	
	THIEN T. MAI	2887	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6 and 9-21* is/are pending in the application.

4a) Of the above claim(s) *15-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement

Acknowledgement is hereby made of Amendment filed 7/06/2009.

Election/Restrictions

1. Newly submitted claims 15-21 are directed to inventions that are independent or distinct from the invention originally claimed for the following reasons: Claims 15-18 are directed to a method comprising the steps of "placing a first substrate on a work surface, placing the chip of the electronic component into a cavity of the first substrate, the conductive areas of the electronic component being applied against the surface of the first substrate, and assembling the first substrate provided with the electronic component on a second substrate provided with conductive tracks, so that the conductive areas of the electronic component applied against the surface of the first substrate connect to the conductive tracks of the second substrate, wherein the conductive areas of the electronic component and the conductive tracks of the second substrate are in contact to achieve an electric connection via a pressure of application of the second substrate on the electronic component, and configured to rub together when repeated stresses are exerted on the substrates". This method is distinct from the invention originally claimed. Furthermore, claims 19-21 are directed to another method comprising the steps of "placing a first substrate on a work surface, placing the chip of the electronic component into a cavity provided with a window cut into a first substrate with a thickness approximately equal to that of the module, the set of fiat contacts shows on the surface level of said first substrate, and assembling the first substrate provided with the electronic component on a second substrate provided with conductive tracks, so that the conductive areas of the opposite face of the electronic component connect to the conductive tracks of the second substrate, wherein the conductive areas of the electronic component and the conductive tracks of the second substrate

are in contact to achieve an electric connection via a pressure of application of the second substrate on the electronic component, and configured to rub together when repeated stresses are exerted on the substrates". This method is also distinct from the invention originally claimed.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 15-21 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim(s) 1-2, 9 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over *Halope* (US 6,851,618).

Re claim 1, *Halope* teaches a process for assembling at least one electronic component made up of a chip provided with contacts on one of the faces of the chip (the Examiner notes that the recitation "said contacts being set off on a conductive film constituting flat conductive areas that extend the contacts of the chip in a plane over the chip, the conductive areas are being connected to conductive tracks placed on a surface of a planar insulating substrate" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to

stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951)), comprising:

placing the substrate on a work surface, the face including conductive tracks 18, 62, 64 (Fig. 1, 4-5) being oriented upwards, placing the electronic component 40 (made up of a chip 26 on a double sided circuit 10 – see Fig. 2, col. 3 lines 18-25) into a cavity of the substrate situated in a zone including the conductive tracks 62, 64, 18, the chip being inserted into the cavity, the conductive areas of the electronic component coming into contact with the corresponding conductive tracks of the substrate, and

applying a layer of insulating material which extends concurrently on the electronic component and at least on the zone of the substrate surrounding said electronic component, wherein the conductive areas of the electronic component and the conductive tracks of the substrate are in contact to achieve an electric connection via a pressure of application of the insulating material layer on the electronic component, and configured to rub together when repeated stressed are exerted on the substrate (col. 4 lines 19-38: electronic component 40 contacts are in connection with antenna without using glue and Fig. 4-6 show the double sided circuit portions of the component 40 are in contact with antenna portions 62, 64 and insulating material covers the entire electronic component 40 and its surrounding; although not expressly described, it would have been obvious that at least a small rubbing/friction would occur at the chip contacts with the antenna while repeated stresses are exerted due to pressure on the electronic component and hot injection of fluid(s) exerting at least a force with pressure while being injected on the surroundings and surface of the component thereby pushing the component around in the cavity thus enabling the component's contact areas to rub with the conductive tracks. It is noted that Figs. 5-6 show little space that would allow the component 40 to be inserted and moved around. Col. 4 lines 22-25 mentions that glue may or may not be

used indicating that there is at least small room or space the component might be moved around but the space is not big enough for the component to lose ohmic connection with the antenna contacts. It is further noted that Halope teaches supports 12, 38 are made with lower Vicat point (col. 4 lines 13-15, col. 3 lines 2-6) such that they become fluidized or softened under hot lamination process. Thus the card of Halope also exhibits an internal deformation during hot lamination which leads to a tendency to push the component around thereby allowing it rub against the conductive tracks).

Re claim 2, *Halope* teaches the electronic component is coated by an insulating material on the face of the chip opposite to the face provided with contacts (see glue 34, 36 in Fig. 2).

Re claim 9, *Halope* teaches the cavity of the electronic component is formed by milling or by stamping a window (col. 3 lines 18+).

3. Claim(s) 6 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over *Halope* (US 6,851,618) in view of *Ikeda* (JP 01020197 A). *Halope*'s teachings have been discussed above.

Halope is unclear with respect to heating the chip before inserting into the cavity.

Ikeda discloses the electronic component is obtained by heating the chip of the electronic component with a mold section 9 resulting in heat dissipation before inserting into the cavity along with aluminum foils 4 (Fig. 1-2, see abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of *Ikeda* for achieving better productivity and production speed by inserting the component into the cavity after being molded while still being warm resulted from the heated mold.

Remarks

Applicant's arguments have been fully considered but they are not persuasive.

In response to applicant's argument that the contact surfaces cannot rub together, it is respectfully submitted that Halope at col. 4 lines 20-25 teaches electronic component 40 contacts are in connection with antenna without using glue and Fig. 4-6 show the double sided circuit portions of the component 40 are in contact with antenna portions 62, 64 and insulating material covers the entire electronic component 40 and its surrounding; although not expressly described, it would have been obvious that at least a small rubbing/friction would occur at the chip contacts with the antenna while repeated stresses are exerted due to pressure on the electronic component and hot injection of fluid(s) exerting at least a force with pressure while being injected on the surroundings and surface of the component thereby pushing the component around in the cavity thus enabling the component's contact areas to rub with the conductive tracks. It is noted that Figs. 5-6 show little space that allows the component 40 to be inserted and moved around. Col. 4 lines 22-25 mentions that glue may or may not be used indicating that there is at least small room or space the component might be moved around but the space is not big enough for the component to lose ohmic connection with the antenna contacts.

Furthermore, Applicant's Fig. 3 shows tight space surrounding the component in the cavity 7 which is also shown in Fig. 5-6 of Halope. Applicant's specification at page 6 lines 5-8 states that "The contact areas of the "lead frame" will have a tendency to rub on the substrate tracks under the action of internal forces produced by the transponder deformation". "Tendency" means that there is a possibility but not definite. It is further noted that Halope teaches supports 12, 38 are made with lower Vicat point (col. 4 lines 13-15, col. 3 lines 2-6) such that they become fluidized or soften under hot lamination process. Thus the card of Halope also exhibits an internal deformation which leads to a tendency to push the component around thereby allowing it rub against the conductive tracks.

For these reasons, the rejection is respectfully maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THIEN T. MAI whose telephone number is (571)272-8283. The examiner can normally be reached on Monday through Friday, 8:00 - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve S. Paik can be reached on 571-272-2404. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thien T Mai/
Examiner, Art Unit 2887

/Thien M. Le/
Primary Examiner, Art Unit 2887